내고장성 임베디드 CPU Core
- Reliable Ultra Low-Power Superscalar Core -

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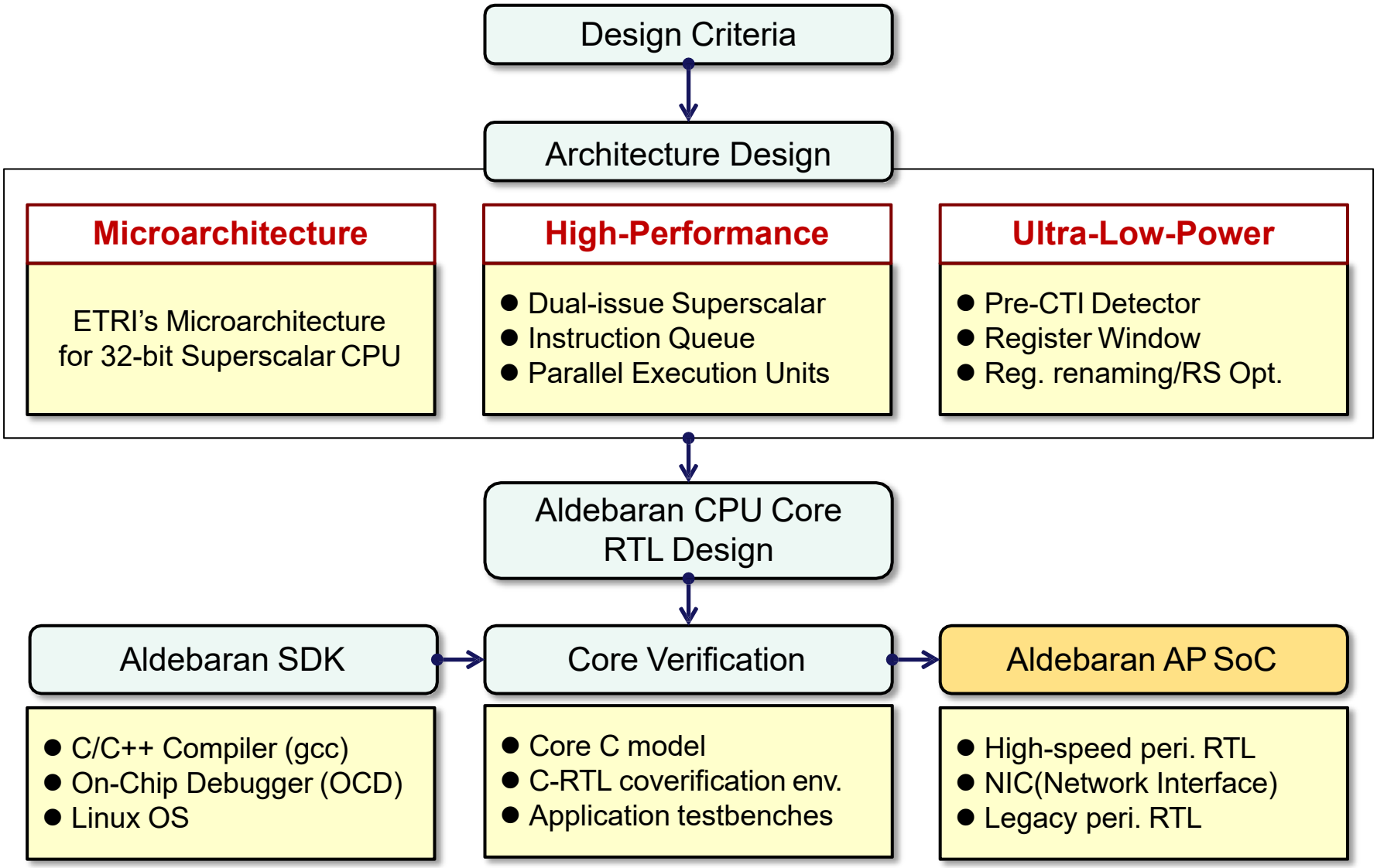
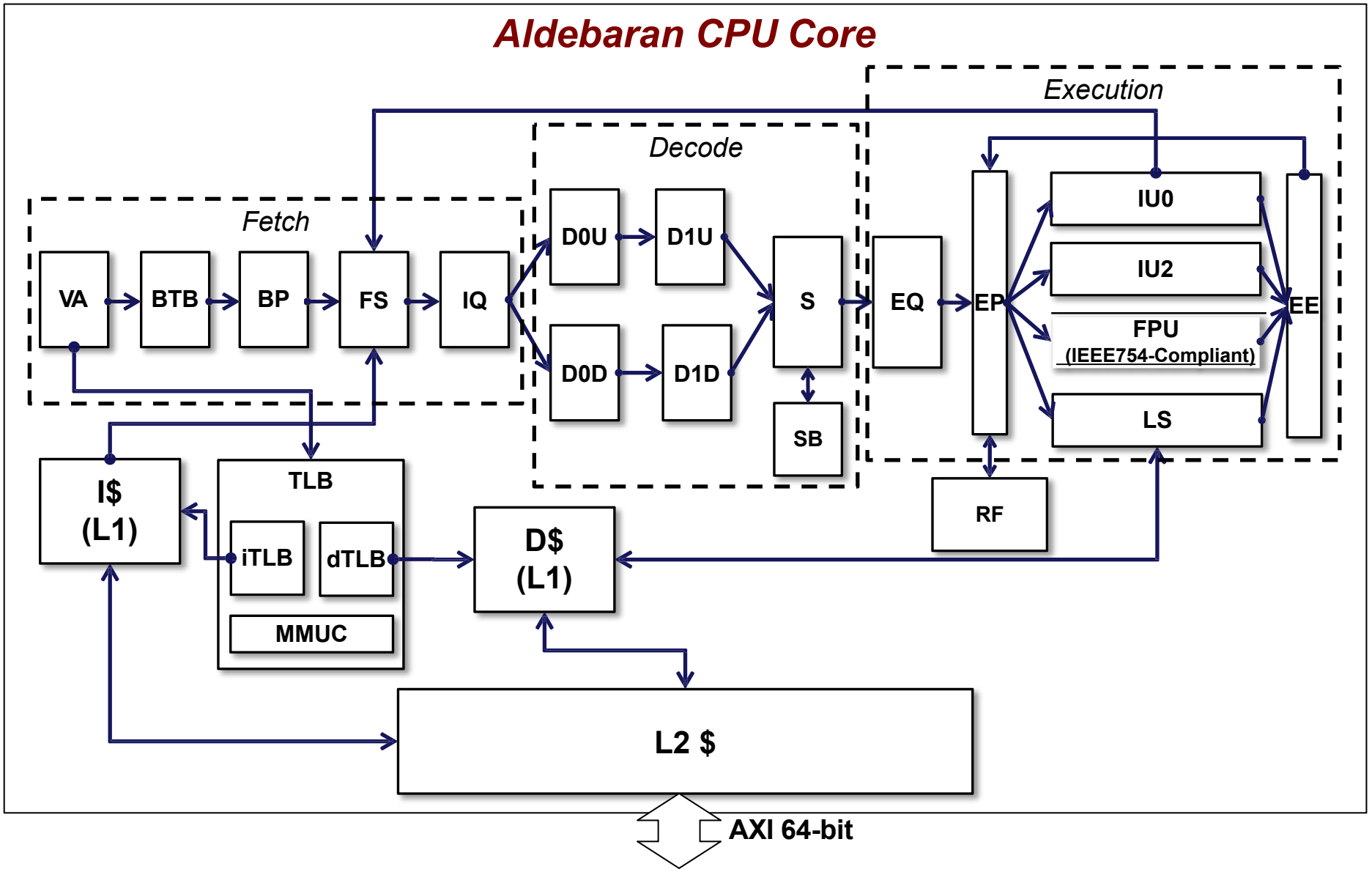
Aldebaran: Ultra Low-Power CPU Core



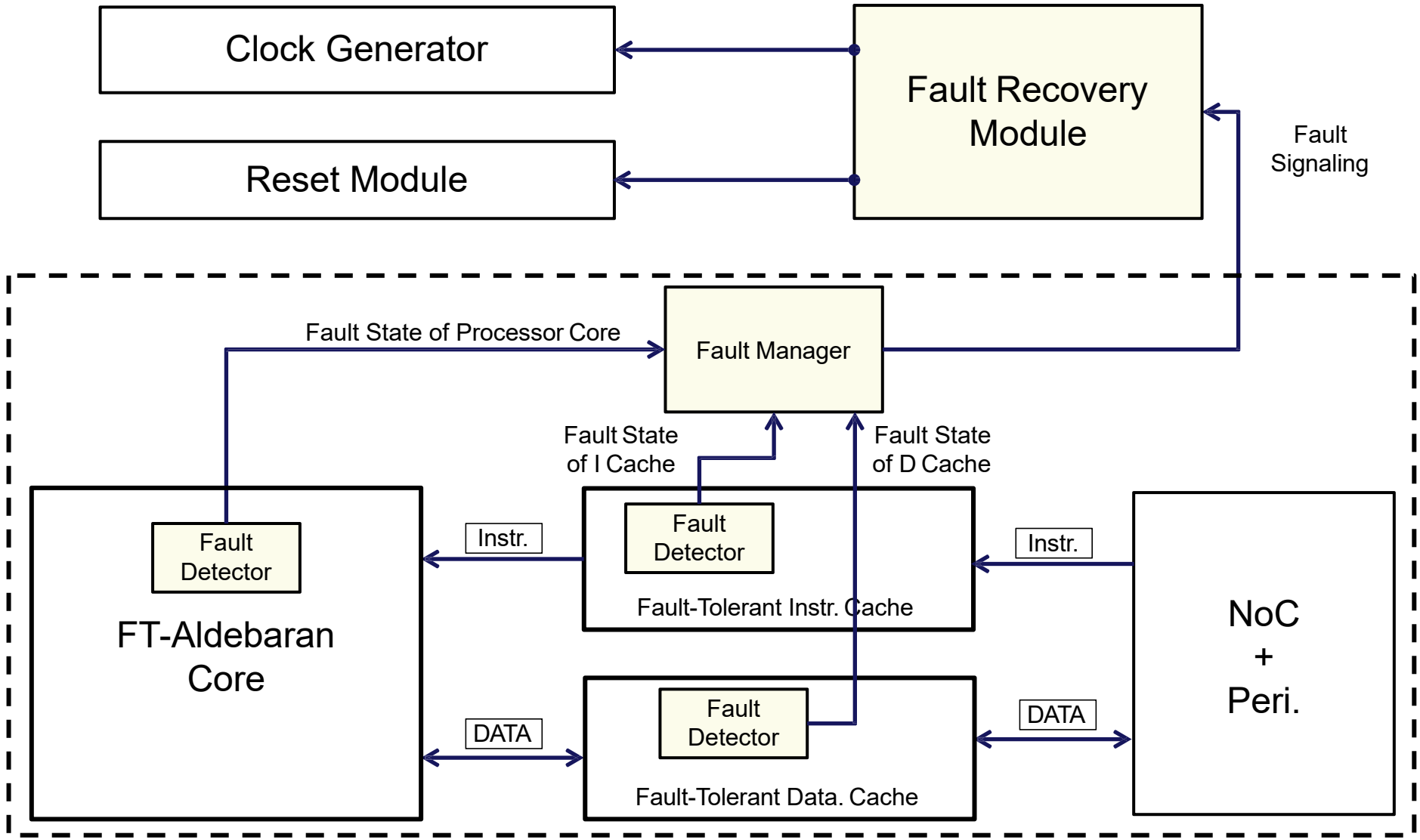
Aldebaran: Ultra Low-Power CPU Core



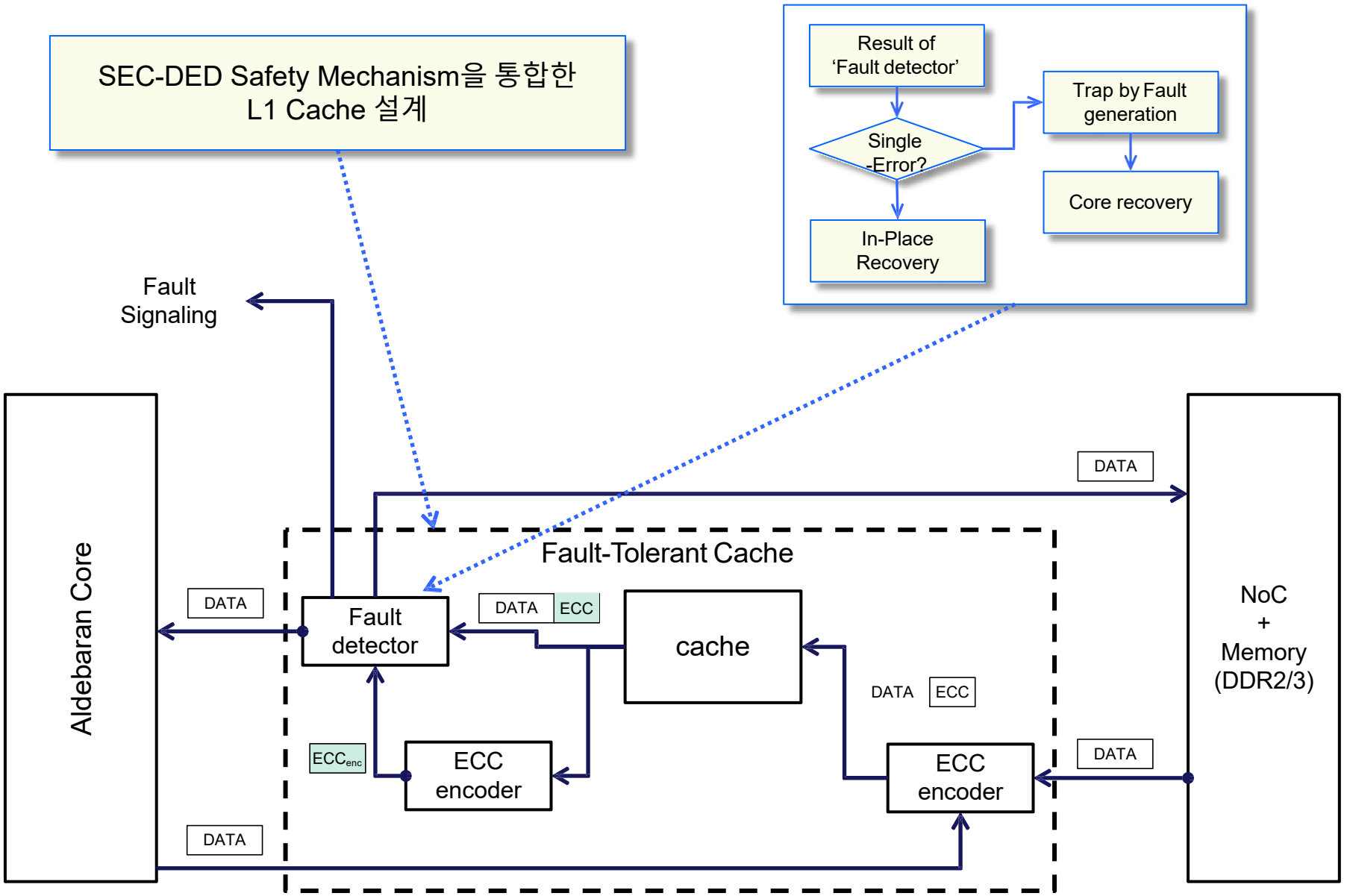
Aldebaran CPU Core Specification

- Dual-issue in-order superscalar with 32bit I/D
- Target : 800MHz@65nm,1.1V, 1GHz@45nm,1.0V
- BTB: 2-way x 256-entry x 58-bit =3.7Kbytes
- BP: 10-bit GHR, 256x16x2b=1Kbyte
- I/D cache: Each 32K bytes, Tag 2.12Kbytes, I$+D$ 68.25Kbytes
- TLB: Each 32-entry PTE(Page Table Entry) for iTLB/dTLB
  - ✓Separate iTLB/dTLB, each 32 entries
  - ✓Each 65-bit PTE with selective FLUSH/PROBE
- Dual-rail decode and in-order scheduler with Scoreboard
- Execution queue
  - ✓Queue containing decoded/scheduled blocks
  - ✓Run-time OS support for LP execution
- Superscalar execution unit
  - ✓2 integer units, 1 load store, and FPU for single/double fpu operations
  - ✓Multi-port register file
- 800MHz, 2.76mm^2@65nm
  c.f) Cortex-A9@45nm의 50% 면적

Fault-Tolerance Architecture



ECC-Protected I/D Cache



Aldebaran SDK

C/C++ Compiler

C/C++ Compiler/Libraries (gcc)

gcc	g++	ar	as	cpp	gcj
gcov	gprof	ld	objcopy	objdump	read_elf
crt1.o	libc	lib pthread	libm	librt	lib stdc++

ADE

Aldebaran Compiler, Eclipse 기반의 Debugger 등을 포함하는 통합 SW 개발 환경

Multi-Core Emulator

Aldebaran 멀티 코어(X8) 100MIPS급 고속 에뮬레이터

※ Core, TLB, 주변장치 모델링
※ Linux Kernel 부팅 속도 : 3초 이내
※ RTL과의 통합 에뮬레이션 지원

OCD

코어(Chip 또는 FPGA)의 JTAG 모듈과 통신하기 위한 Server Software
※ OCD : On-Chip Debugger

EEMBC Benchmark

COREMARK® An EEMBC Benchmark

FPMARK™ An EEMBC Benchmark

Drivers

Timer


LCD with TS


Audio


Memory


NAND Flash


Camera

UART


Ethernet

JTAG

Debugger

C/C++ Source-Level Debugging을 위한 Client Software

OS (Linux, RTEMS)

Kernel_3.3 Linux

RTEMS

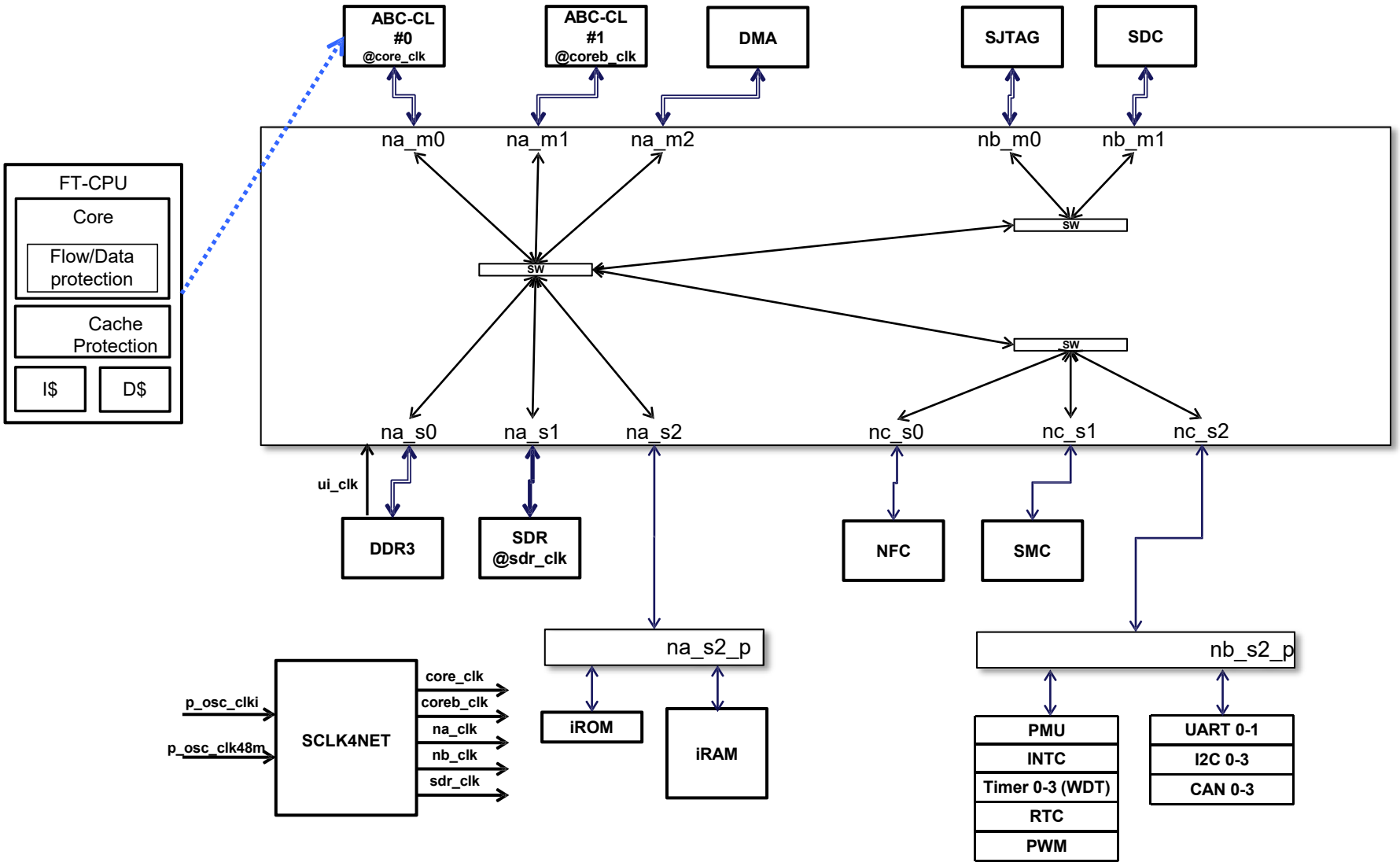
Monitor

SoC내의 HW Probing 및 주변 장치를 제어하기 위한 SW

Applications

Multimedia, Vision, Detection, Recognition, Qt등 다양한 App. 을 통한 컴파일러 및 코어 기능 검증

Fault Tolerant SoC Architecture

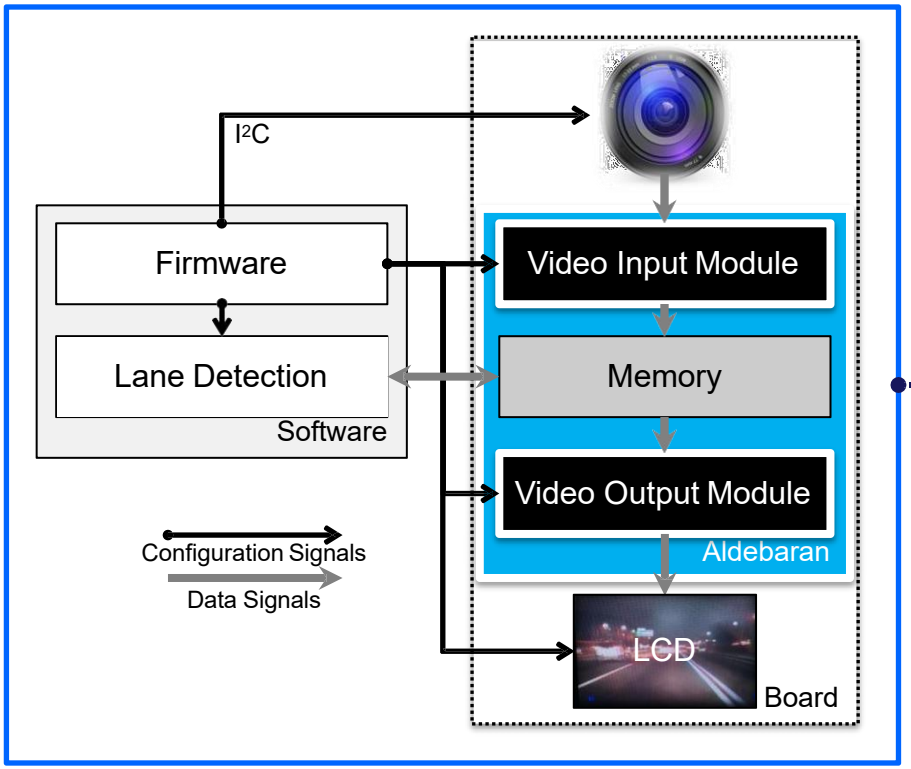


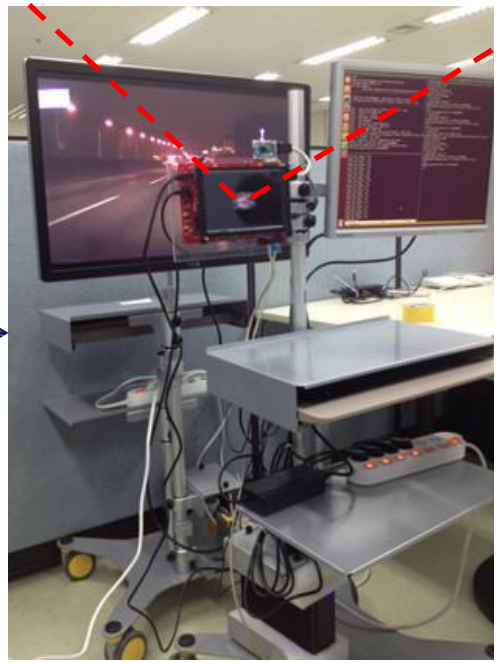
Aldebaran Boards

AB-F7(or F6) Board

AB-F7A Board

LDWS Architecture and Experiments





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방식 (택 1)		조건[1)]
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